EPCOS

Data Book 2008

CeraDiode for ESD Protection

www.epcos.com

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EPCOS

Contents

EPCOS

Contents

Overview of series

Series	Case size inch/mm	EPCOS type	Semiconductor diode package	$V_{DC,max}$ V	C_{typ} pF
Single standard	0402/1005	CDS2...GTA	SOD-723	5.6; 15	47; 180
	0603/1608	CDS3...GTA	SOD-523	5.6 ... 22	56 ... 470
	1003/2508	CDS4...GTA	SOD-323	12	82
Array standard	0508/1220	CDA4...GTA	-	22	33
	0612/1632	CDA5...GTA	-	22	56
Single high-speed	0402/1005	CDS2...HDMI1	SOD-723	5.6	0.6
	0402/1005	CDS2...GTH	SOD-723	15; 16	2; 10
	0603/1608	CDS3...HDMI1	SOD-523	5.6	0.6
	0603/1608	CDS3...GTH	SOD-523	16; 30	3; 10
	1003/2508	CDS4...GTH	SOD-323	16	3
Array high-speed	0508/1220	CDA4...GTH	-	16	10
	0612/1632	CDA5...GTH	-	16	3
	1012/2532	CDA6...GTH	SOT-23 6L	5.6	7

1 Description

Due to ongoing miniaturization, today's electronic devices are more and more sensitive to electrostatic discharge (ESD). That makes reliable protection components absolutely necessary to safeguard valuable electronics against the impact of ESD.

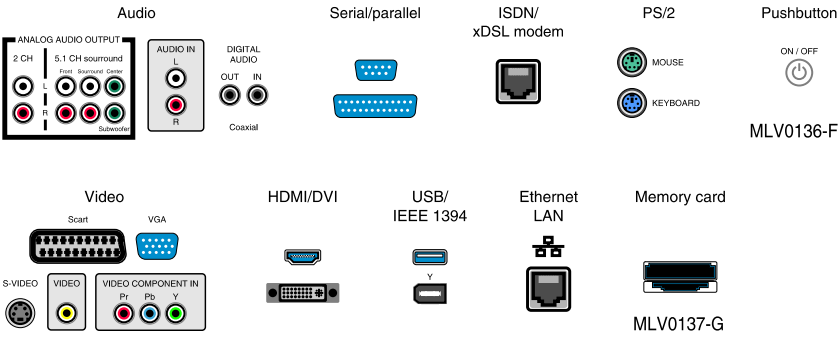
1. CeraDiodes are ceramic semiconductor components optimized for **ESD protection** of data, audio and video lines, ICs and I/O ports in electronic devices.
2. CeraDiodes are (cost-effective) alternatives to semiconductor protection devices such as Zener and TVS diodes. In many cases, the CeraDiode is a 1:1 replacement for these devices (F.F.F. = fit, form, function).
3. CeraDiodes have a nonlinear voltage/current characteristic for effectively suppressing extremely fast voltage transients and offer superior parametric stability over the complete operating range of –40 °C to +85 °C.
4. CeraDiodes are bidirectional devices. A single CeraDiode connected from a signal/data line to ground routes both positive and negative ESD transitions safely to the ground plane. This technique eliminates the need to route ESD charge into the power plane, possibly damaging nearby integrated circuits. CeraDiodes for high-speed lines exhibit a very low capacitance designed for maximum ESD protection combined with minimal signal distortion.

2 Applications

- Consumer products (TV, DVD player/recorder, set-top box, game consoles, MP3 player, digital still/video camera, etc.)
- EDP products (desktop and notebook computer, monitor, PDA, printer, memory card, etc.)
- Peripherals (control unit, headset, speaker, drive, etc.)
- Industrial
- Mobile communication (SIM card, etc.)
- etc.

3 Interfaces

- Video
- Audio
- USB
- IEEE 1394 (Firewire, DV, etc.)
- Ethernet
- DVI
- HDMI
- Parallel/serial
- SATA
- Pushbuttons
- etc.



Interfaces protected against ESD by CeraDiode (examples)

Application matrix

				Video analog (Scart, Composite, Component, S-Video, VGA)	DVI	HDMI	Audio analog	Audio digital	USB 1.1 / 2.0	IEEE 1394 (Firewire, DV, i.Link)	Ethernet	Serial port	Parallel port	LCD data line	Disk drive, hard disk drive	SATA	Memory card, SIM card	Bluetooth	Analog modem / ISDN	xDSL modem	WLAN	Keyboard, pushbutton, PS/2
Devices	Case size inch/mm	EPCOS type	Semi-diode package																			
Single standard	0402/1005	CDS2C05GTA	SOD-723				x					x							x			x
	0402/1005	CDS2C15GTA	SOD-723				x		x[1)]	x[1)]		x							x			x
	0603/1608	CDS3C05GTA	SOD-523				x					x							x			x
	0603/1608	CDS3C09GTA	SOD-523				x					x							x			x
	0603/1608	CDS3C15GTA	SOD-523				x		x[1)]	x[1)]		x							x			x
	0603/1608	CDS3C20GTA	SOD-523				x					x							x			x
	1003/2508	CDS4C12GTA	SOD-323				x		x[1)]	x[1)]		x							x			x
Array standard	0508/1220	CDA4C20GTA	-				x	x				x							x			x
	0612/1632	CDA5C20GTA	-				x	x				x							x			x
Single high-speed	0402/1005	CDS2C05HDMI1	SOD-723		x	x			x	x	x						x				x	
	0402/1005	CDS2C15GTH	SOD-723	x				x	x	x			x	x	x		x	x		x	x	
	0402/1005	CDS2C16GTH	SOD-723	x	x			x	x	x	x		x	x	x	x	x	x		x	x	
	0603/1608	CDS3C05HDMI1	SOD-523		x	x			x	x	x					x					x	
	0603/1608	CDS3C16GTH	SOD-523	x	x			x	x	x	x		x	x	x	x	x	x		x	x	
	0603/1608	CDS3C30GTH	SOD-523	x				x	x	x			x	x	x		x	x		x	x	
	1003/2508	CDS4C16GTH	SOD-323	x	x			x	x	x	x		x	x	x	x	x	x		x	x	
Array high-speed	0508/1220	CDA4C16GTH	-	x				x	x	x			x	x	x		x	x		x	x	
	0612/1632	CDA5C16GTH	-	x	x			x	x	x	x		x	x	x	x	x	x		x	x	
	1012/2532	CDA6C05GTH	SOT-23 6L	x				x	x	x	x		x		x	x	x	x		x	x	

[1)] Supply line

MLV0190-V-E

1 Difference between the characteristic curves of semiconductor diodes and CeraDiodes

Semiconductor diodes

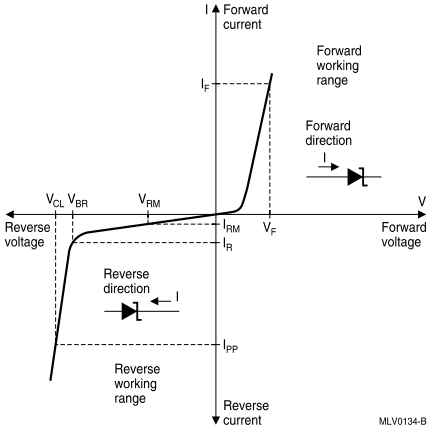


Figure 1: Characteristic curve of semiconductor diodes

CeraDiodes

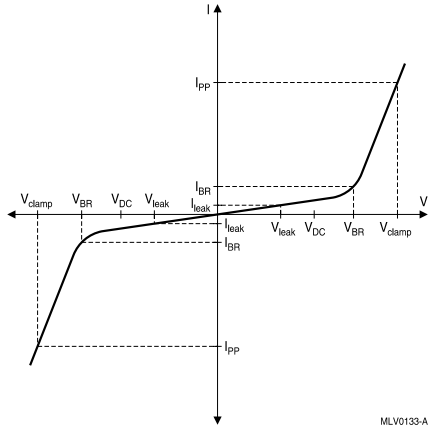


Figure 2: Characteristic curve of CeraDiodes

1.1 Leakage current

@ Semiconductor diode

A semiconductor diode is normally operated in the reverse direction (reverse working range). In normal use the diode has such a huge internal resistance that almost no current can flow through it. As the resistance is not infinite, however, a small current known as the leakage current I_{RM} flows through the diode. This leakage current is specified at a defined voltage V_{RM}.

@ CeraDiode

As the CeraDiode is a bidirectional component it can be used in both forward and reverse directions with no difference. During normal operation the internal resistance of the CeraDiode is so huge that almost no current can flow through it. As the resistance is not infinite, however, a small current known as the leakage current I_{leak} flows through the diode. This current is specified at a defined voltage V_{leak}.

1.2 Maximum operating voltage

@ Semiconductor diode

The voltage V_{RM} resembles the maximum acceptable operating voltage. The current I_{RM} that flows is called the leakage current.

@ CeraDiode

V_{DC} is the maximum operating voltage that can be applied to the CeraDiode. To minimize the leakage current, the maximum applied voltage should be in the V_{leak} range.

1.3 Breakdown voltage

@ Semiconductor diode

If the diode voltage increases, e.g. due to an ESD pulse, the diode breaks down at the breakdown voltage V_{BR}. A current I_R then flows through the diode. The breakdown voltage V_{BR} is specified with a current I_R = 1 mA.

@ CeraDiode

If the diode voltage increases, e.g. due to an ESD pulse, the CeraDiode breaks down at a breakdown voltage V_{BR}. A current I_R then flows through the diode. The breakdown voltage V_{BR} is specified at a current of I_R = 1 mA.

1.4 Clamping voltage

@ Semiconductor diode

The diode restricts the overvoltage, which may be caused by an ESD pulse on the clamping voltage. This is the voltage that would drop across the diode in the event of an overvoltage. To describe the clamping behavior of the diode, the voltage V_{CL} is specified with a current I_{PP} = 1 A. It is designated as the clamping voltage in the glossary.

@ CeraDiode

The diode restricts the overvoltage, which may be caused by an ESD pulse on the clamping voltage. This is the voltage that would drop across the diode in the event of an overvoltage. To describe the clamping behavior of the diode, the voltage V_{clamp} is specified with a current I_{PP} = 1 A. It is designated as the clamping voltage.

1.5 Forward working range

@ Semiconductor diode

As the semiconductor diode is a unidirectional component, it can be used even in forward direction (forward working range). When the diode operates in this range (e.g. for negative overvoltage pulses) it has to be ensured that the current through the diode does not exceed the maximum specified forward current. This current may have to be limited with a series resistor. In this operating range, the diode is characterized by the forward voltage V_F and the current I_F.

@ CeraDiode

Being a bidirectional component, the CeraDiode can be operated forward or reverse biased, forward operation corresponding to reverse operation. There is no forward working range.

1.6 Symbols and terms - CeraDiode versus semiconductor diode

CeraDiode	Semiconductor diode	
C_{typ}		Typical capacitance
I_{BR}	I_R, I_T	(Reverse) current @ breakdown voltage
I_{leak}	I_{RM}	(Reverse) leakage current
I_{PP}	I_{PP}	Current @ clamping voltage
I_{PP}	I_P, I_{PP}	Peak pulse current
P_{PP}	P_{PP}	Peak pulse power
V_{BR}	V_{BR}	(Reverse) breakdown voltage
V_{clamp}	$V_{cl,}$ V_C	Clamping voltage
V_{DC}	V_{RM}, V_{RWM}, V_{WM}, V_{DC}	(Reverse) stand-off voltage, working voltage, operating voltage
V_{leak}	V_{RM}, V_{RWM}, V_{WM}, V_{DC}	(Reverse) voltage @ leakage current
- *)	I_F	Current @ forward voltage
- *)	I_{RM}, $I_{RM,max}$@V_{RM}	(Reverse) current @ maximum reverse stand-off voltage, working voltage, operating voltage
- *)	V_F	Forward voltage

*) Not applicable due to bidirectional characteristics of CeraDiodes

1 Bidirectional ESD protection to IEC 61000-4-2 (level 4)

All CeraDiodes satisfy requirements to the IEC 61000-4-2 international ESD standard, level 1 to 4 and are tested within the scope of the human body model (330 Ω/150 pF).

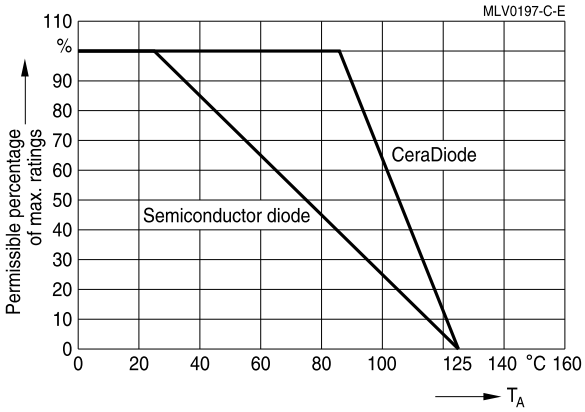
- Designed for uni and bidirectional lines
- Routes all ESD events, both positive and negative, safely to ground
- Suitable for DC working voltages up to 30 V

Single and array surface mount package in case sizes

- single 0402 (semiconductor package SOD-723)
- single 0603 (semiconductor package SOD-523)
- single 1003 (semiconductor package SOD-323)
- array 0508 (no equivalent semiconductor package available)
- array 0612 (no equivalent semiconductor package available)
- array 1012 (semiconductor package SOT23-6L)

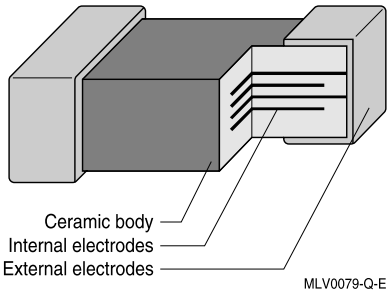
2 No change in ESD protection performance at temperatures >25 °C

Because they contain millions of pn-junctions, CeraDiodes offer a huge volume for energy absorption. This results in constant high ESD protection performance up to 85 °C. In contrast, semiconductor diodes have only one pn-junction for energy absorption. Their ESD protection performance thus declines after 25 °C.

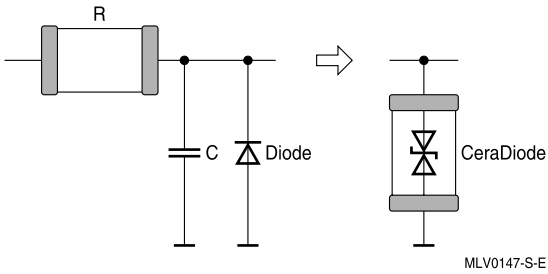


3 Use of parasitic capacitance for RFI suppression and high-frequency filtering (replacement of additional MLCC)

Thanks to their construction with internal electrodes, CeraDiodes offer both ESD protection and sufficient capacitance for RFI suppression and high-frequency filtering. One CeraDiode can replace a semiconductor diode and a capacitor. Its high-frequency behaviour is similar to a C0G ceramic capacitor. Moreover, there is no need for a series resistor to limit the current. The CeraDiode consequently saves both space and costs.



Cross-section through a CeraDiode



Resistor + capacitor + semiconductor diode replaced by one CeraDiode

4 Surge current capability

CeraDiodes are designed for ESD protection. Depending on their individual construction, however, some of them (CeraDiode standard series) can also withstand surge currents. The maximum permissible ratings for surge-current and thus for energy absorption of these surge-current-capable devices depend on the pulse shape, pulse duration and the number of times this load is repeated during the overall lifetime. CeraDiodes designed to handle surge current have in most cases greater surge-current capability than semiconductor diodes.

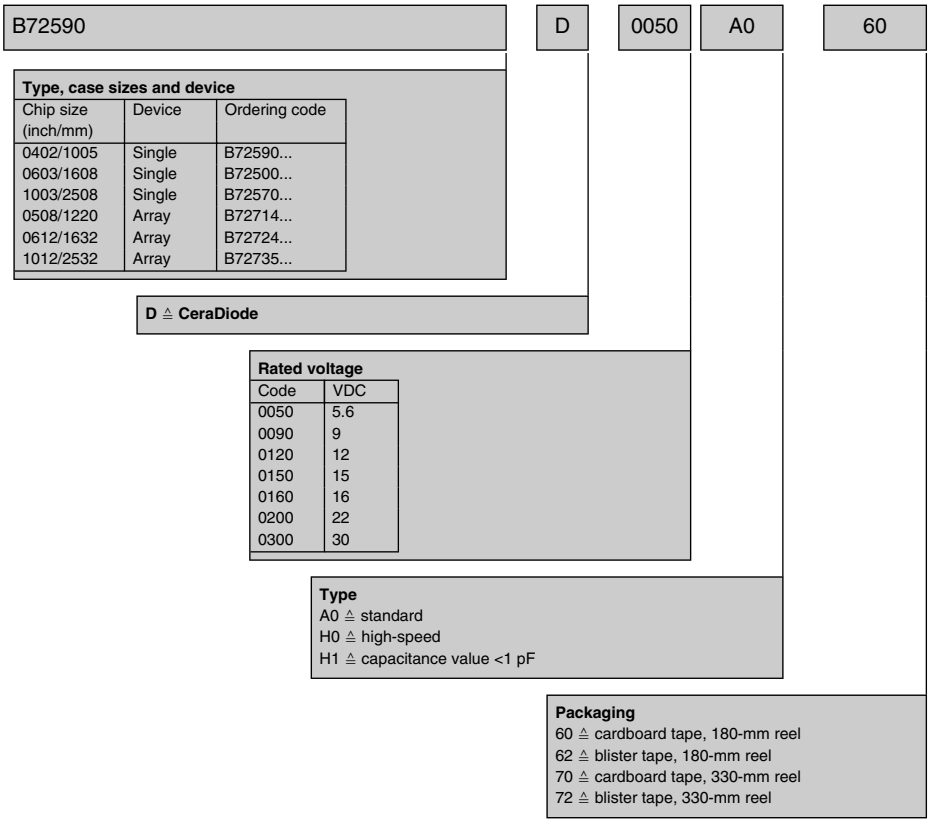
5 Low parasitic inductance

Semiconductor diodes are soldered to a board by wire tags. These can produce high parasitic inductance, which in turn has a significant influence on the clamping voltage of the diode (the higher the parasitic inductance, the higher the clamping voltage). The CeraDiode has no such wire terminals, i.e. any parasitic inductance is much smaller, and with that its influence on the clamping voltage is also reduced.

6 Further features

- Low leakage current
- Fast response time <0.5 ns
- Lead-free nickel barrier terminations suitable for lead-free soldering
- RoHS-compatible

EPCOS ordering code system



EPCOS type designation

CD	S	2	C05	GTA

CD ≙ CeraDiode

Device
S ≙ Single device
A ≙ Array device

Case sizes of single devices

Code	Case size (inch/mm)
2	0402/1005
3	0603/1608
4	1003/2508

Case sizes of array devices

Code	Case size (inch/mm)
4	0508/1220
5	0612/1632
6	1012/2532

Rated voltage

Code	VDC
05	5.6
09	9
12	12
15	15
16	16
20	22
30	30

Type
GTA ≙ standard
GTH ≙ high-speed
HDMI1 ≙ capacitance value <1 pF

CeraDiodes

Standard series

SMD

Single chip:

4-fold array:

Features

- ESD protection to IEC 61000-4-2, level 4
- Bidirectional ESD protection in one component
- No change in ESD protection performance at temperatures up to 85 °C
- Use of parasitic capacitance for RFI suppression and high-frequency filtering (replacement of additional MLCC)
- High surge current capability
- Low parasitic inductance
- Low leakage current
- Fast response time <0.5 ns
- Lead-free nickel barrier terminations suitable for lead-free soldering
- RoHS-compatible

Applications

- Interfaces, data lines, power lines and audio lines, pushbuttons, serial ports, ICs and I/O ports
- Consumer electronic products (TV, DVD player/recorder, set-top box, game consoles, MP3 player, digital still/video camera, etc.)
- EDP products (desktop and notebook computer, monitor, PDA, printer, memory card, control unit, head set, speaker, HDD, optical drive, etc.)
- Industrial applications

Construction

- Multilayer technology
- Nickel barrier termination (Ag/Ni/Sn) for lead-free soldering

Delivery mode

- Cardboard and blister tape, 180-mm reel (blister for case size 0612), 330-mm reel on request

General technical data

Maximum DC operating voltage		$V_{DC,max}$	5.6 ... 22	V
Typical capacitance		C_{typ}	33 ... 470	pF
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Leakage current[1)]	(V_{leak} = 5.6 V)	I_{leak}	1	µA
Operating temperature	(without derating)	T_{op}	−40/+85	°C
Storage temperature		T_{stg}	−40/+125	°C

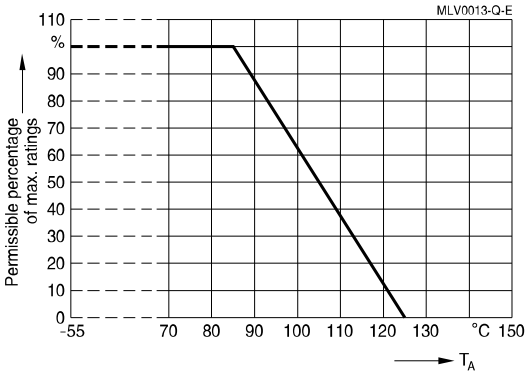
1) Except CDS2C05GTA and CDS3C05GTA V_{leak} = 3.3 V. Any operating voltage lower than V_{leak} results in lower leakage current.

SMD

Electrical specifications and ordering codes
Maximum ratings ($T_{op,max}$ = 85 °C) and characteristics (T_A = 25 °C)

Type	Ordering code	$V_{DC,max}$ V	$V_{BR,min}$ (1 mA) V	$V_{clamp,max}$ (1 A) V	I_{PP} (8/20 µs) A	P_{PP} (8/20 µs) W	C_{typ} (1 MHz, 1 V) pF
Array, 4-fold, case size 0508, no semiconductor diode equivalent							
CDA4C20GTA	B72714D0200A060	22	24	60	10	600	33
Array, 4-fold, case size 0612, no semiconductor diode equivalent							
CDA5C20GTA	B72724D0200A062	22	25	50	30	2200	56
Single, case size 0402, SOD-723							
CDS2C05GTA	B72590D0050A060	5.6	6.4	24	10	320	180[1)]
CDS2C15GTA	B72590D0150A060	15	20	46	10	670	47
Single, case size 0603, SOD-523							
CDS3C05GTA	B72500D0050A060	5.6	6.4	19	30	1000	470[1)]
CDS3C09GTA	B72500D0090A060	9	10	30	30	1600	220[1)]
CDS3C15GTA	B72500D0150A060	15	22	42	30	2000	160[1)]
CDS3C20GTA	B72500D0200A060	22	25	50	30	2200	56
Single, case size 1003, SOD-323							
CDS4C12GTA	B72570D0120A060	12	16	46	20	1000	82

Typical characteristics

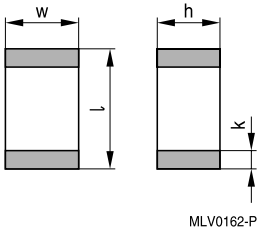


1) C_{typ} measured at V = 1 V, f = 1 kHz.

SMD

Dimensional drawings

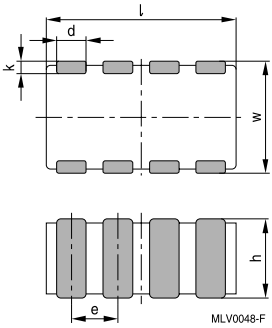
Single device



Dimensions in mm

Case size (inch) (mm)	0402 1005		0603 1608		1003 2508	
	Min.	Max.	Min.	Max.	Min.	Max.
l	0.85	1.15	1.45	1.75	2.34	2.74
w	0.4	0.6	0.7	0.9	0.7	0.9
h	0.4	0.6	0.7	0.9	0.7	0.9
k	0.1	0.3	0.1	0.4	0.13	0.75

Array device



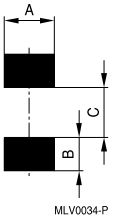
Dimensions in mm

Case size (inch) (mm)	0508 1220		0612 1632	
	Min.	Max.	Min.	Max.
l	1.8	2.2	3.0	3.4
w	1.05	1.45	1.45	1.75
h	-	0.9	-	0.9
d	0.2	0.4	0.25	0.55
e	0.4	0.6	0.61	0.91
k	-	0.35	-	0.35

SMD

Recommended solder pads

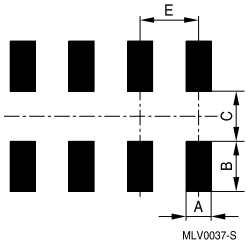
Single device



Recommended dimensions in mm

Case size	(inch) (mm)	0402 1005	0603 1608	1003 2508
A		0.6	1.0	0.8
B		0.6	1.0	0.8
C		0.5	1.0	1.45

Array device



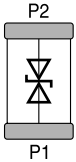
Recommended dimensions in mm

Case size	(inch) (mm)	0508 1220	0612 1632
A		0.35	0.5
B		0.9	0.7
C		0.4	1.2
E		0.5	0.76

SMD

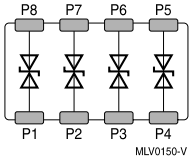
Pin configurations

Single device



Pin	Description
P1	GND
P2	I/O line

Array device

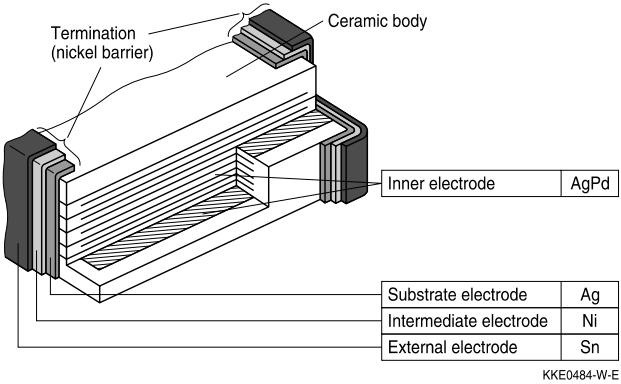


Pin	Description
P1	GND
P2	GND
P3	GND
P4	GND
P5	I/O line 1
P6	I/O line 2
P7	I/O line 3
P8	I/O line 4

SMD

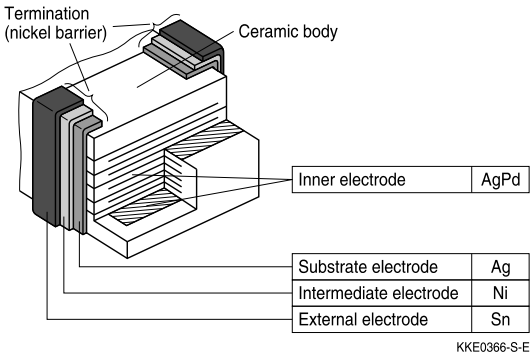
Termination

Single device



KKE0484-W-E

Array device



KKE0366-S-E

CeraDiodes

High-speed series

SMD

Single chip:

4-fold array:

2/4 data + 1 supply:

Features

- Very low capacitance values 0.6 up to 10 pF
- ESD protection to IEC 61000-4-2, level 4
- Bidirectional ESD protection in one component
- No change in ESD protection performance at temperatures up to 85 °C
- Use of parasitic capacitance for RFI suppression and high-frequency filtering (replacement of additional MLCC)
- Low parasitic inductance
- Low leakage current
- Fast response time <0.5 ns
- Lead-free nickel barrier terminations suitable for lead-free soldering
- RoHS-compatible

Applications

- Interfaces, data lines (USB, IEEE 1394, Ethernet, parallel port, SATA, etc.), audio lines (digital) and video lines (analog), DVI, HDMI, ICs and I/O ports
- Consumer electronic products (TV, DVD player/recorder, set-top box, game consoles, MP3 player, digital still/video camera, etc.)
- EDP products (desktop and notebook computer, monitor, PDA, printer, memory card, control unit, head set, speaker, HDD, optical drive, etc.)
- Industrial applications

Construction

- Multilayer technology
- Nickel barrier termination (Ag/Ni/Sn) for lead-free soldering

Delivery mode

- Cardboard and blister tape, 180-mm reel (blister for case sizes 0612 and 1012), 330-mm reel on request

General technical data

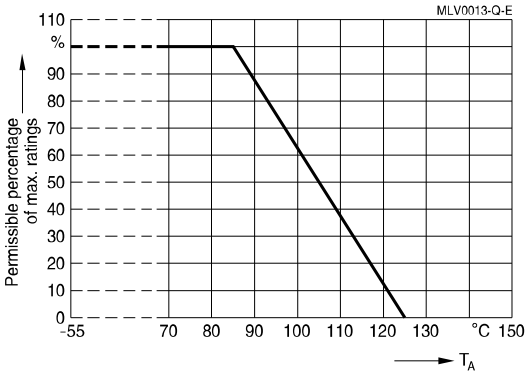
Maximum DC operating voltage		$V_{DC,max}$	5.6 ... 30	V
Typical capacitance		C_{typ}	0.6 ... 10	pF
Air discharge ESD capability	to IEC 61000-4-2	$V_{ESD,air}$	15	kV
Contact discharge ESD capability	to IEC 61000-4-2	$V_{ESD,contact}$	8	kV
Leakage current	(V_{leak} = 5.6 V)	I_{leak}	1	µA
Operating temperature		T_{op}	−40/+85	°C
Storage temperature		T_{stg}	−40/+125	°C

SMD

Electrical specifications and ordering codes
Maximum ratings ($T_{op,max}$ = 85 °C) and characteristics (T_A = 25 °C)

Type	Ordering code	$V_{DC,max}$ V	$V_{BR,min}$ (1 mA) V	$V_{clamp,max}$ (1 A) V	C_{typ} (1 MHz, 1 V) pF
Array, 2/4 data + 1 supply, case size 1012, SOT-23 6L					
CDA6C05GTH	B72735D0050H062	5.6	52	195	7
Array, 4-fold, case size 0508, no semiconductor diode equivalent					
CDA4C16GTH	B72714D0160H060	16	22	66	10
Array, 4-fold, case size 0612, no semiconductor diode equivalent					
CDA5C16GTH	B72724D0160H062	16	80	350	3
Single, case size 0402, SOD-723					
CDS2C05HDMI1	B72590D0050H160	5.6	150	-	0.6
CDS2C15GTH	B72590D0150H060	15	23	66	10
CDS2C16GTH	B72590D0160H060	16	65	290	2
Single, case size 0603, SOD-523					
CDS3C05HDMI1	B72500D0050H160	5.6	150	-	0.6
CDS3C16GTH	B72500D0160H060	16	65	290	3
CDS3C30GTH	B72500D0300H060	30	50	120	10
Single, case size 1003, SOD-323					
CDS4C16GTH	B72570D0160H060	16	38	146	3

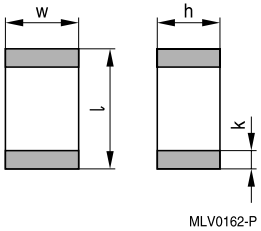
Typical characteristics



SMD

Dimensional drawings

Single device



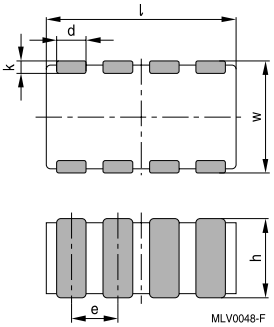
MLV0162-P

Dimensions in mm

Case size (inch) / (mm)	0402 / 1005		0603 / 1608		1003 / 2508	
	Min.	Max.	Min.	Max.	Min.	Max.
l	0.85	1.15	1.45	1.75	2.34	2.74
w	0.4	0.6	0.7	0.9	0.7	0.9
h	0.4	0.6	0.7	0.9	0.7	0.9
k	0.1	0.3	0.1	0.4	0.13	0.75

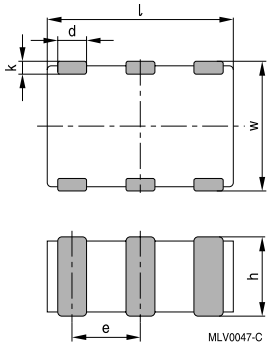
Array devices

4-fold array



MLV0048-F

2/4 data + 1 supply



MLV0047-C

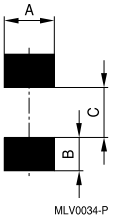
Dimension in mm

Case size (inch) / (mm)	0508 / 1220		0612 / 1632		1012 / 2532	
	Min.	Max.	Min.	Max.	Min.	Max.
l	1.8	2.2	3.0	3.4	2.90	3.50
w	1.05	1.45	1.45	1.75	2.25	2.75
h	-	0.9	-	0.9	-	1.2
d	0.2	0.4	0.25	0.55	0.35	0.65
e	0.4	0.6	0.61	0.91	0.8	1.1
k	-	0.35	-	0.35	-	0.45

SMD

Recommended solder pads

Single device

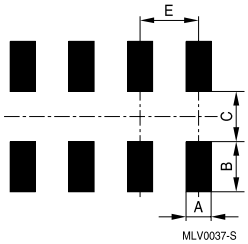


Recommended dimensions in mm

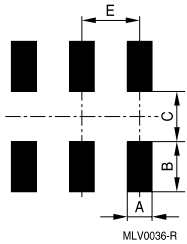
Case size (inch) / (mm)	0402 / 1005	0603 / 1608	1003 / 2508
A	0.6	1.0	0.8
B	0.6	1.0	0.8
C	0.5	1.0	1.45

Array devices

4-fold array



2/4 data + 1 supply



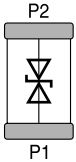
Recommended dimensions in mm

Case size (inch) / (mm)	0508 / 1220	0612 / 1632	1012 / 2532
A	0.35	0.5	0.7
B	0.9	0.7	1.0
C	0.4	1.2	1.4
E	0.5	0.76	0.95

SMD

Pin configurations

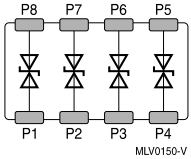
Single device



Pin	Description
P1	GND
P2	I/O line

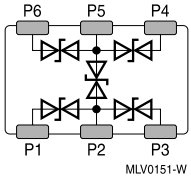
Array devices

4-fold array



Pin	Description
P1	GND
P2	GND
P3	GND
P4	GND
P5	I/O line 1
P6	I/O line 2
P7	I/O line 3
P8	I/O line 4

2/4 data + 1 supply

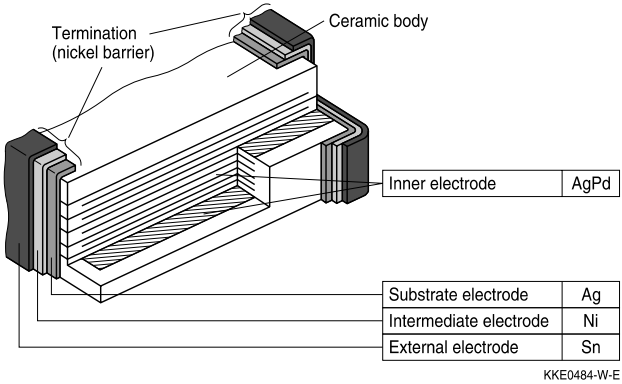


Pin	Description
P1	I/O line 1
P2	GND
P3	I/O line 2
P4	I/O line 3
P5	V_{DC}
P6	I/O line 4

SMD

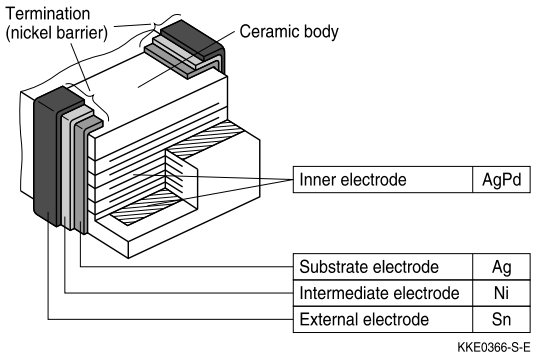
Termination

Single device



KKE0484-W-E

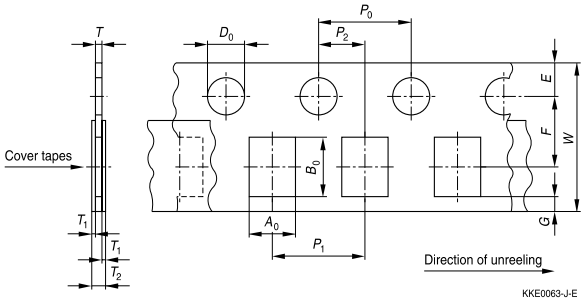
Array device



KKE0366-S-E

1 Taping and packing for chip and array CeraDiodes

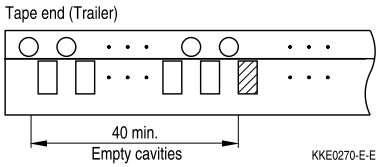
1.1 Cardboard tape (taping to IEC 60286-3)

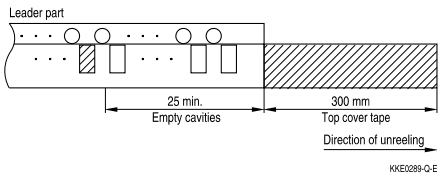


Dimensions in mm

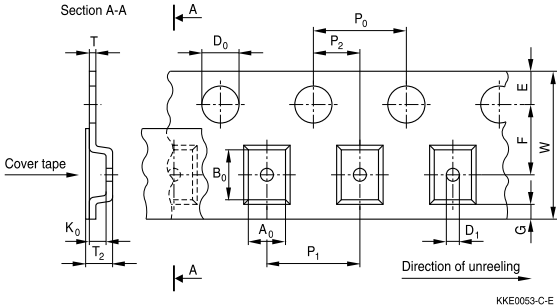
Case size (inch) (mm)		0402 1005	0603 1608	1003 2508	0508 1220	Tolerance
Compartment width	A_0	0.6	0.95	1.0	1.6	±0.2
Compartment length	B_0	1.15	1.8	2.85	2.4	±0.2
Sprocket hole diameter	D_0	1.5	1.5	1.5	1.5	+0.1/ −0
Sprocket hole pitch	P_0	4.0	4.0	4.0	4.0	±0.1[1)]
Distance center hole to center compartment	P_2	2.0	2.0	2.0	2.0	±0.05
Pitch of component compartments	P_1	2.0	4.0	4.0	4.0	±0.1
Tape width	W	8.0	8.0	8.0	8.0	±0.3
Distance edge to center of hole	E	1.75	1.75	1.75	1.75	±0.1
Distance center hole to center compartment	F	3.5	3.5	3.5	3.5	±0.05
Distance compartment to edge	G	0.75	0.75	0.75	0.75	min.
Thickness tape	T	0.6	0.9	1.0	0.95	max.
Overall thickness	T_2	0.7	1.1	1.1	1.12	max.

[1)] ≤ ±0.2 mm over 10 sprocket holes





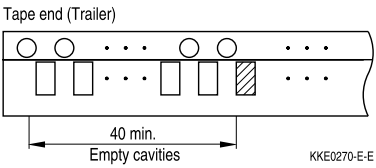
1.2 Blister tape (taping to IEC 60286-3)

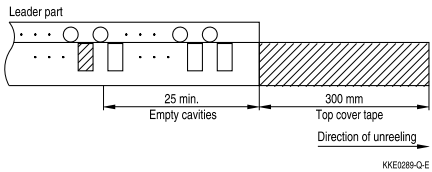


Dimensions in mm

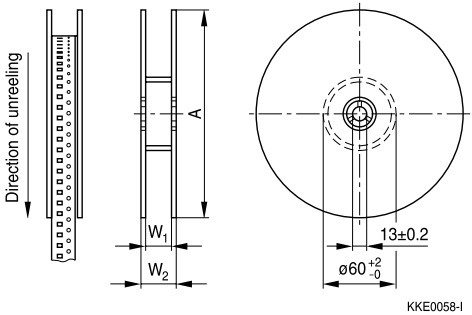
Case size (inch) (mm)		**0612** **1632**	**1012** **2532**	**Tolerance**
Compartment width	A_0	1.9	2.8	±0.2
Compartment length	B_0	3.5	3.5	±0.2
Compartment height	K_0	1.8	1.8	max.
Sprocket hole diameter	D_0	1.5	1.5	+0.1/ −0
Compartment hole diameter	D_1	1.0	1.0	min.
Sprocket hole pitch	P_0	4.0	4.0	±0.1[1)]
Distance center hole to center compartment	P_2	2.0	2.0	±0.05
Pitch of component compartments	P_1	4.0	4.0	±0.1
Tape width	W	8.0	8.0	±0.3
Distance edge to center of hole	E	1.75	1.75	±0.1
Distance center hole to center compartment	F	3.5	3.5	±0.05
Distance compartment to edge	G	0.75	0.75	min.
Thickness tape	T	0.3	0.3	max.
Overall thickness	T_2	2.5	2.5	max.

[1)] ≤ ±0.2 mm over 10 sprocket holes





1.3 Reel packing



Dimensions in mm

		Dimensions	Tolerance	Dimensions	Tolerance
Reel diameter	A	180	+0/ –3	330	±2
Reel width (inside)	W_1	8.4	+1.5/ –0	8.4	+1.5/ –0
Reel width (outside)	W_2	14.4	max.	14.4	max.

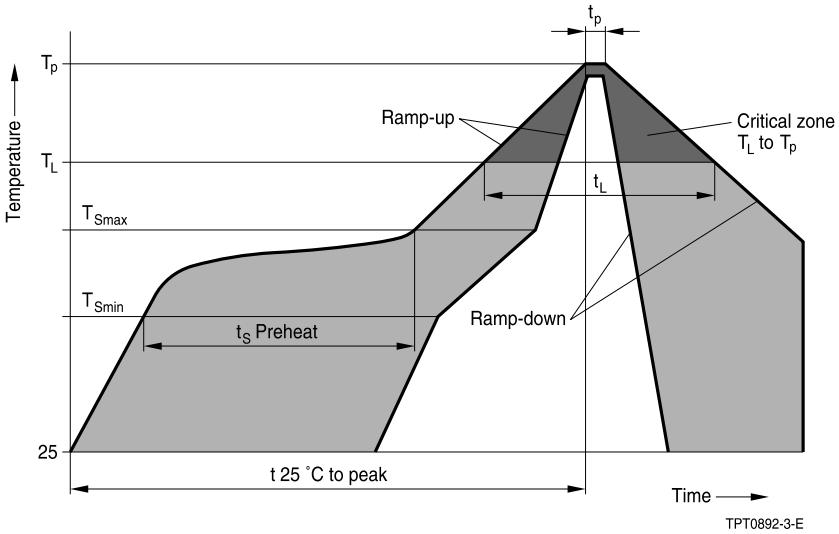
Package: 8-mm tape
Reel material: Plastic

1.4 Packing units

Case size (inch) / (mm)	∅ 180-mm reel pieces	∅ 330-mm reel pieces	Tape
0402 / 1005	10000	50000	cardboard
0603 / 1608	4000	16000	cardboard
1003 / 2508	4000	16000	cardboard
0508 / 1220	4000	16000	cardboard
0612 / 1632	3000	12000	blister
1012 / 2532	2000	8000	blister

1 Recommended infrared soldering temperature profile

Recommended temperature characteristic following JEDEC J-STD-020C



Profile feature	Sn-Pb eutectic assembly	Pb-free assembly
Average ramp-up rate (T_{Smax} to T_p)	3 °C / s max.	3 °C / s max.
Preheat		
– Temperature min (T_{Smin})	100 °C	150 °C
– Temperature max (T_{Smax})	150 °C	200 °C
– Time (t_{Smin} to t_{Smax})	60 … 120 s	60 … 180 s
Time maintained above:		
– Temperature min (T_L)	183 °C	217 °C
– Time (t_L)	60 … 150 s	60 … 150 s
Peak/classification temperature (T_p)	220 °C … 240 °C	245 °C … 260 °C
Time within 5 °C of actual peak temperature (t_p)	10 … 30 s	20 … 40 s
Ramp-down rate	6 °C / s max.	6 °C / s max.
Time 25 °C to peak temperature	6 min max.	8 min max.

Note: All temperatures refer to the top side of the package, measured on the package body surface.

2 Soldering guidelines

The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.

The components are suitable for reflow soldering to JEDEC J-STD-020C.

3 Solder joint profiles / solder quantity

3.1 Cement quantity

The component is fixed onto the circuit board with cement prior to soldering. It must still be able to move slightly. When the board is placed into the reflow oven, excessively rigid fixing can lead to high forces acting on the component and thus to a break. In addition, too much cement can lead to unsymmetrical stressing and thus to mechanical fracture of the component. The cement must also be so soft during mounting that no mechanical stressing occurs.

3.2 Mounting the components on the board

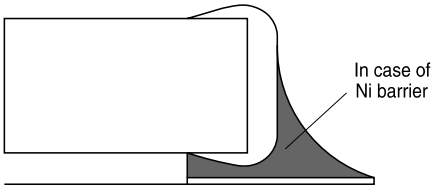
It is best to mount the components on the board before soldering so that one termination does not enter the oven first and the second termination is soldered subsequently. The ideal case is simultaneous wetting of both terminations.

3.3 Solder joint profiles

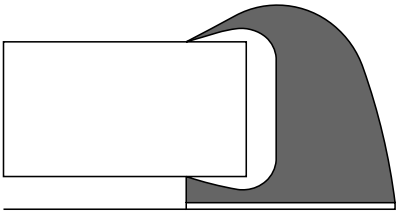
If the meniscus height is too low, that means the solder quantity is too low, the solder joint may break, i.e. the component becomes detached from the joint. This problem is sometimes interpreted as leaching of the external terminations.

If the solder meniscus is too high, i.e. the solder quantity is too large, the vise effect may occur. As the solder cools down, the solder contracts in the direction of the component. If there is too much solder on the component, it has no leeway to evade the stress and may break, as in a vise.

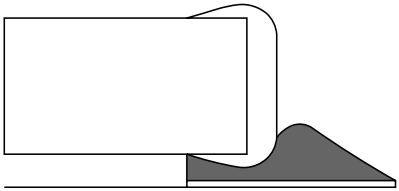
3.3.1 Solder joint profiles for nickel barrier termination



Good solder joint MLV0196-B-E



Too much solder
Pad geometry too large KKE0071-A-E



Poor wetting KKE0072-I-E

Good and poor solder joints caused by amount of solder in infrared reflow soldering

4 Solderability tests

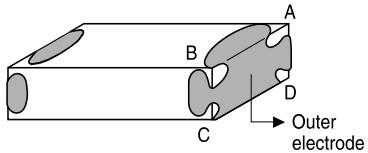
Test	Standard	Test conditions / Sn-Pb soldering	Test conditions / Pb-free soldering	Criteria / test results
Wettability	IEC 60068-2-58	Immersion in 60/40 SnPb solder using non-activated flux at 215 ±3 °C for 3 ±0.3 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux at 245 ±5 °C for 3 ±0.3 s	Covering of 95% of end termination, checked by visual inspection
Leaching resistance	IEC 60068-2-58	Immersion in 60/40 SnPb solder using mildly activated flux without preheating at 255 ±5 °C for 10 ±1 s	Immersion in Sn96.5Ag3.0Cu0.5 solder using non- or low activated flux without preheating at 255 ±5 °C for 10 ±1 s	No leaching of contacts
Tests of resistance to soldering heat for SMDs	IEC 60068-2-58	Immersion in 60/40 SnPb for 10 s at 260 °C	Immersion in Sn96.5Ag3.0Cu0.5 for 10 s at 260 °C	Capacitance change: $-15\% \leq \Delta C \leq 15\%$

Note:

Leaching of the termination

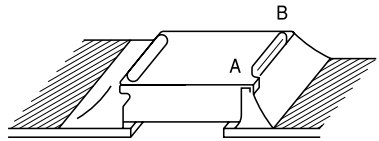
Effective area at the termination might be lost if the soldering temperature and/or immersion time are not kept within the recommended conditions. Leaching of the outer electrode should not exceed 25% of the chip end area (full length of the edge A-B-C-D) and 25% of the length A-B, shown below as mounted on the substrate.

As single chip



KKE0312-T-E

As mounted on substrate



KKE0313-2

5 Notes for proper soldering

5.1 Preheating and cooling

- The average ramp-up rate must not exceed 3 °C/s.
- The cooling rate must not exceed 8 °C/s.

5.2 Repair / rework

Manual soldering with a soldering iron must be avoided, hot-air methods are recommended for making repairs.

5.3 Cleaning

All environmentally compatible agents are suitable for cleaning. Select the appropriate cleaning solution according to the type of flux used. The temperature difference between the components and cleaning liquid must not be greater than 100 °C. Ultrasonic cleaning should be carried out with the utmost caution. Too high ultrasonic power can impair the adhesive strength of the metallized surfaces. Insufficient or excessive cleaning can be detrimental to CeraDiode performance.

5.4 Solder paste printing (reflow soldering)

An excessive application of solder paste results in too high a solder fillet, thus making the chip more susceptible to mechanical and thermal stress. This will lead to the formation of cracks. Too little solder paste reduces the adhesive strength on the outer electrodes and thus weakens the bonding to the PCB. The solder should be applied smoothly to the end surface to a height of min. 0.2 mm.

5.5 Selection of flux

Used flux should have less than or equal to 0.1 wt % of halogenated content, since flux residue after soldering could lead to corrosion of the termination and/or increased leakage current on the surface of the CeraDiode. Strong acidic flux must not be used. The amount of flux applied should be carefully controlled, since an excess may generate flux gas, which in turn is detrimental to solderability.

5.6 Storage

Solderability is guaranteed for one year from date of delivery, provided that components are stored in their original packages.

Storage temperature: −25 °C to +45 °C

Relative humidity: ≤75% annual average, ≤95% on 30 days a year

The solderability of the external electrodes may deteriorate if SMDs are stored where they are exposed to high humidity, dust or harmful gas (hydrogen chloride, sulfurous acid gas or hydrogen sulfide).

Do not store SMDs where they are exposed to heat or direct sunlight. Otherwise the packing material may be deformed or SMDs may stick together, causing problems during mounting.

After opening the factory seals, such as polyvinyl-sealed packages, it is recommended to use the SMDs as soon as possible.

5.7 Placement of components on circuit board

It is of advantage to place the components on the board before soldering so that their two terminals do not enter the solder oven at different times. Ideally, both terminals should be wetted simultaneously.

5.8 Soldering caution

- Sudden heating or cooling of the component results in thermal destruction by cracks.
- An excessively long soldering time or high soldering temperature results in leaching of the outer electrodes, causing poor adhesion due to loss of contact between electrodes and termination.
- Avoid manual soldering with a soldering iron.
- Wave soldering must not be applied for CeraDiodes designated for reflow soldering only.
- Keep to the recommended down-cooling rate.

5.9 Standards

CECC 00802
IEC 60068-2-58
IEC 60068-2-20
JEDEC J-STD-020C

1 Microstructure and conduction mechanism

CeraDiodes are bidirectional transient voltage suppressor devices made of ceramic oxides and built with a multilayer structure. Each layer consists of numerous ZnO grains. Each point of contact between the zinc and oxide grains thus acts as a micro CeraDiode, comparable to a Zener diode. The large number of micro CeraDiodes makes this component much more rugged with respect to ESD then a semiconductor diode, which has only one available pn-junction.

Sintering zinc oxide together with other metal oxide additives under specific conditions produces a polycrystalline ceramic whose resistance shows strong dependence on voltage.

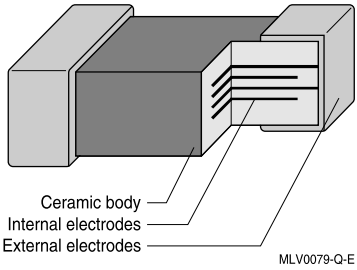


Figure 1

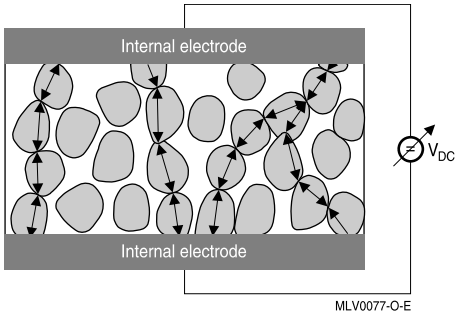


Figure 2

Figures 1 and 2: Internal structure of a CeraDiode

Figure 2 shows a simplified form of the conduction mechanism of the EPCOS CeraDiode. The zinc oxide grains themselves are highly conductive, whereas the inter-granular boundary formed from other oxides is highly resistive. Only at the contact points of zinc oxide grains does the sintering produce “micro pn-junctions”, comparable to symmetrical Zener diodes (protection level approx. 3.5 V).

The electrical behavior of the CeraDiode results from the number of micro pn-junctions connected in series or in parallel. The physical dimensions of the CeraDiode determine its electrical properties:

- Twice the ceramic thickness produces twice the protection level because twice as many micro pn-junctions are arranged in series.
- Twice the area produces twice the current handling capability because twice the number of current paths are arranged in parallel.
- Twice the volume produces almost twice the energy absorption capability because there are twice as many absorbers in the form of zinc oxide grains.

The series and parallel connection of the individual micro pn-junctions in the sintered body also explains its high electrical load capacity compared to normal semiconductors. Whereas the power in semiconductors is dissipated almost entirely in the thin pn-junction area, in a CeraDiode it is distributed over the entire oxide, i.e. uniformly throughout the component volume. Each oxide contains energy absorbers in the form of zinc oxide grains with optimum thermal contact. This permits high absorption of energy and thus exceptionally high surge current handling capability.

Another advantage of the inner structure of the CeraDiodes is that their parasitic inductances are very low, which results in response times of < 0.5 ns. Semiconductor diodes have a greater parasitic inductance, with typical response times of between 0.8 and 3 ns.

The shape, thickness and number of internal electrodes can be varied to achieve the electrical characteristics required to satisfy individual customer needs.

2 ESD (standard to IEC 61000-4-2)

The trend towards even smaller components and ever lower signal levels increases the susceptibility of electronic circuits to interference due to electrostatic disturbance. Simply touching the device may lead to electrostatic discharge causing functional disturbance with far-reaching consequences even to the point of component breakdown. Studies have shown that the human body can be charged up to 15 kV on an insulated floor (e.g. synthetic fiber carpeting).

In order to safeguard immunity to interference and thus ensure CE compliance, measures are needed to prevent damage due to electrostatic discharge (ESD). This applies to both the circuit layout and to the selection of suitable overvoltage protection.

IEC 61000-4-2 describes the test procedures and specifies various severity levels:

IEC 61000-4-2 Test Level	Test voltage (contact discharge)	Test voltage (air discharge)
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

Figure 3 shows the discharge circuit and Figure 4 the waveform of the discharge current with an extremely short rise time of 0.7 to 1.0 ns and amplitudes of up to 45 A. Secondary effects caused by this edge steepness are high electrical and magnetic field strengths.

In the ESD test, at least ten test pulses are applied with the polarity to which the device under test is most sensitive.

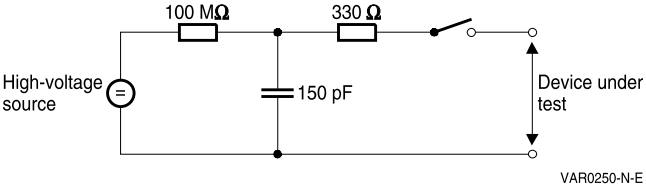


Figure 3: ESD discharge circuit to IEC 61000-4-2

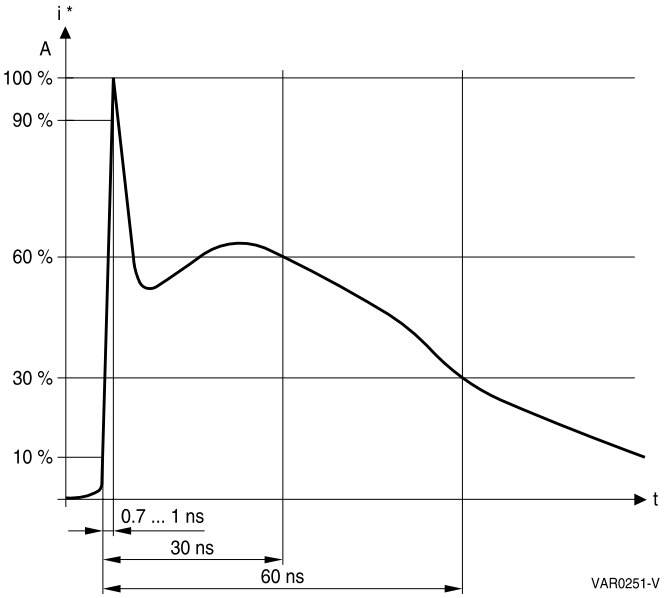


Figure 4: ESD discharge current to IEC 61000-4-2

3 Temperature derating of CeraDiodes

Derating is the intentional reduction of maximum ratings in the application of a device. CeraDiodes are derated at higher operating temperatures as they offer a huge volume for energy absorption due to their millions of pn-junctions. This results in constant high ESD protection performance up to 85 °C. In contrast, semiconductor diodes have only one pn-junction for energy absorption. Their ESD protection performance thus declines after 25 °C.

For operating temperatures exceeding 85 °C the following operating conditions of CeraDiodes

- voltage
- surge current
- energy absorption

have to be derated according to Figure 5.

Figure 5 also shows the advantage of CeraDiodes over semiconductor diodes. Derating already starts at 25 °C for the latter, whereas it starts only after 85 °C for CeraDiodes.

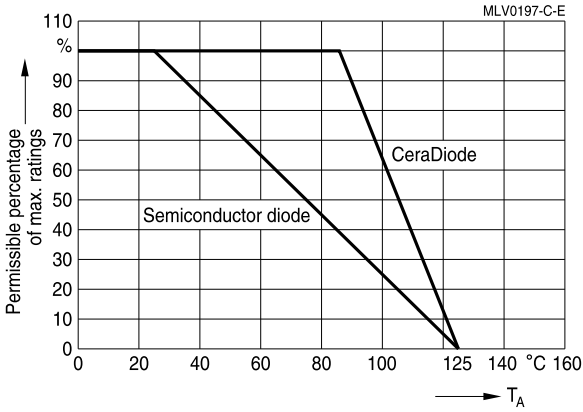


Figure 5: Temperature derating for CeraDiodes and semiconductor diodes

4 Surge current capability of CeraDiodes

CeraDiodes are designed for ESD protection. Depending on their individual construction, however, some CeraDiodes can also cope with surge current.
In the latter case, the maximum permissible ratings for surge current and thus for energy absorption depend on the pulse shape, pulse duration and the number of times this load is repeated during the overall lifetime for both CeraDiodes and semiconductor diodes. CeraDiodes designed to handle surge current have in most cases greater surge current capability than semiconductor diodes, as shown in Figure 6.

Figure 6 shows the change of reverse breakdown voltage V_{BR} @ 1 mA over increasing surge current (8/20 µs pulse) for a single CeraDiode CDS4C12GTA and a single semiconductor diode from a competitor (assessment criterion: breakdown voltage V_{BR} @ 1 mA and operating voltage $V_{DC,max}$ = 12 V as limit).
The breakdown voltage V_{BR} @ 1 mA of the semiconductor diode degrades after a surge current pulse of 20 A and the diode is destroyed. In contrast, the CeraDiode has a constant breakdown voltage of V_{BR} @ 1 mA up to 35 A.

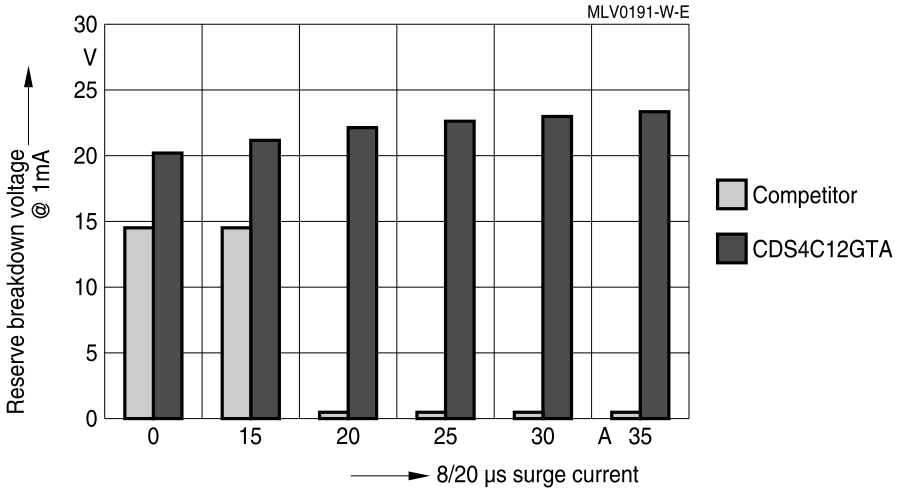


Figure 6: Surge current capability of CeraDiodes and semiconductor diodes in comparison

For surge current capability of CeraDiodes, see data sheet.

Electronic systems and circuits containing integrated circuits (IC) are sensitive to overvoltage transients such as ESD (electrostatic discharge) pulses. These pulses can enter an electrical device when the port is touched or its connector is removed. Ports and connectors are probably the most common routes through which an ESD pulse can be introduced into a device. The pulse travels through the connector to the PC board. It then propagates down the data and/or supply lines to the components on the board. Without sufficient protection, these components may become inoperable or even be destroyed. In view of their great importance, ICs are of special concern to be protected.

The CeraDiodes listed in this chapter satisfy the typical requirements normally required by these applications. The customer has to test and approve parts in the application.

1 Video and audio

Despite the advent of digital interfaces such as DVI and HDMI, it is still the case that TV and DVD sets, set-top boxes, etc. are most commonly linked by SCART, S-video, composite or component connectors. Video and audio connectors need ESD protection to prevent the destruction of downstream electronics due to the sensitivity of the ICs. Depending on the application, video and audio lines are connected via a single group of interfaces comprising S-video / composite video / audio connectors.

1.1 Video lines

Requirements of the CeraDiode:

- ESD protection to IEC 61000-4-2
- Low capacitance to prevent signal distortion

For suitable CeraDiodes, see chapter "Application matrix".

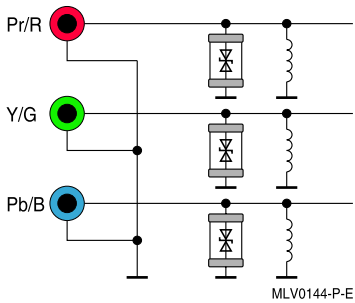
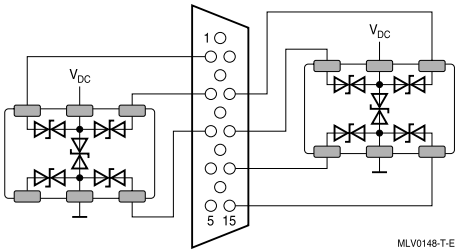


Figure 1 : CeraDiode protection for component / RGB video line

VGA ports are typical analog video connectors between computers and monitors. ESD protection is required for the graphic controller connected to the VGA port.



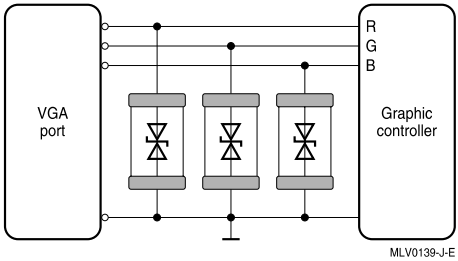


Figure 2 Figure 3

Figures 2 and 3: CeraDiodes for graphic controller protection at the VGA port

1.2 Audio lines

CeraDiodes satisfy the typical requirements on audio line protection devices for ESD and EMI in a single component.

Requirements of the CeraDiode:

- ESD protection to IEC 61000-4-2
- High-frequency noise filtering for high-quality audio signals
- Bidirectional operation and low line capacitance for the digital audio system

For suitable CeraDiodes, see chapter "Application matrix".

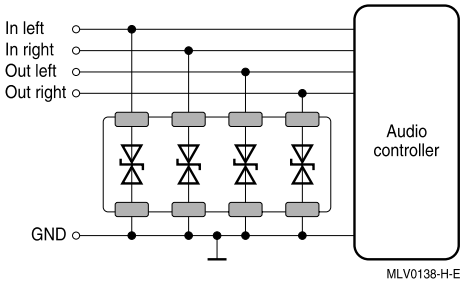


Figure 4: Four ports can be protected with a single array component (e.g. CDA5C20GTA)

To obtain high-quality audio signals, high-frequency noise must be filtered out. CeraDiodes handle both RFI suppression and ESD protection. So it is sufficient for the application to use a single CeraDiode instead of a semiconductor diode and a capacitor. By using an array, up to four ports can be protected with a single component.

The audio leads in a digital audio system (e.g. Dolby Digital, DTS) cannot be protected by a unidirectional diode, as this would drive the negative component of the audio signal to saturation. CeraDiodes are even more attractive here thanks to their bidirectional operation. In contrast, the alternative bidirectional TVS diodes are large and expensive. Thanks to their bidirectional protection and integrated capacitance, CeraDiodes are the ideal protection for audio applications.

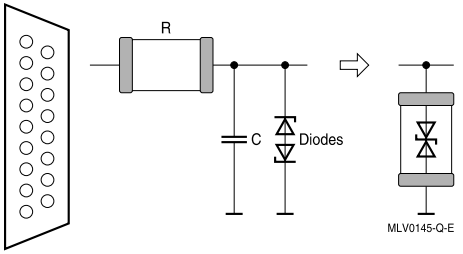


Figure 5:
Protection of audio lines (e.g. in SCART connector) with CeraDiodes

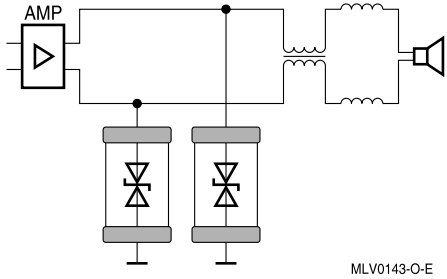


Figure 6:
Audio line and EMI protection in a single component for headset application with CeraDiodes, e.g. CDS3C05GTA (470 pF)

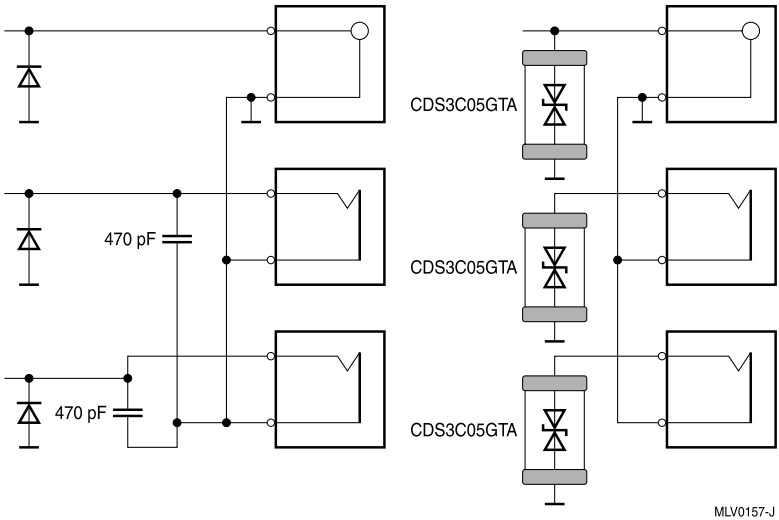


Figure 7: Protection of RCA connectors and audio lines with semiconductor diodes + capacitors (left) and CeraDiodes (right). Note the space saving due to fewer components.

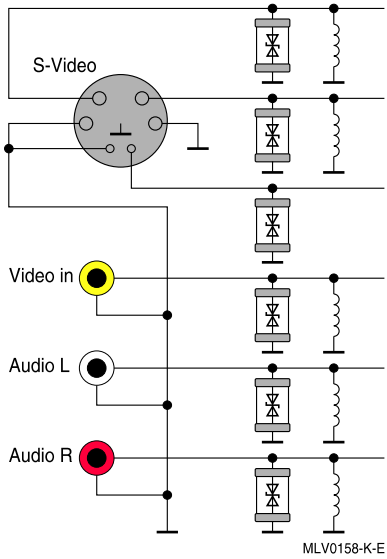


Figure 8: Protection of the S-video, composite video and analog audio group with CeraDiodes

2 USB

The universal serial bus (USB) has become the standard interface for data systems. As data and consumer electronics have merged, USB has spread into more and more electronic devices. The USB is extremely sensitive to ESD. Data rates of up to 480 Mbit/s require a very low line capacitance to avoid signal distortion.

Requirements of the CeraDiode:

- ESD protection for high-speed data transmission to IEC 61000-4-2, level 4
- EMI filtering
- Very low capacitance to prevent signal distortion on the data line

For suitable CeraDiodes, see chapter "Application matrix".

Single port protection

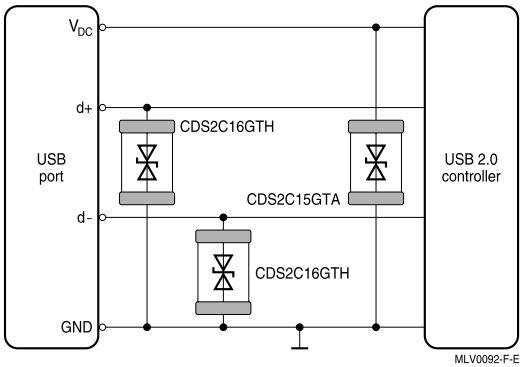


Figure 9: USB 2.0 single port protection with single CeraDiodes

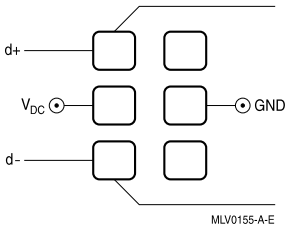


Figure 10

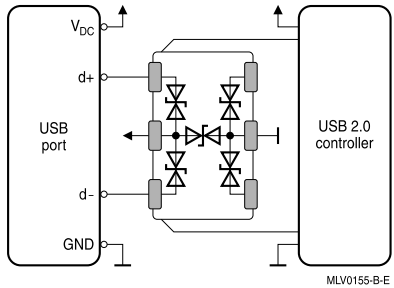


Figure 11

Figures 10 and 11: USB 2.0 single port protection with a high-speed array CDA6C05GTA

Dual port protection

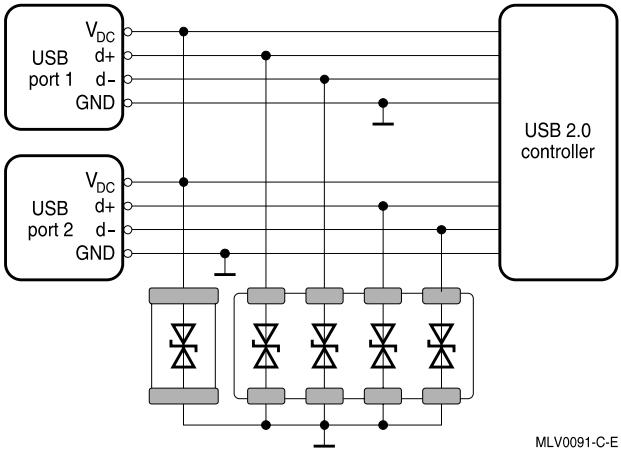


Figure 12: USB 2.0 dual port protection with a single component (e.g. CDS2C15GTA) and an array (e.g. CDA5C16GTH)

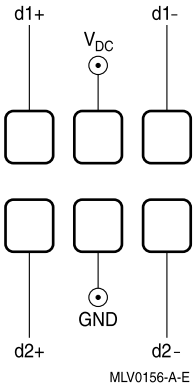


Figure 13

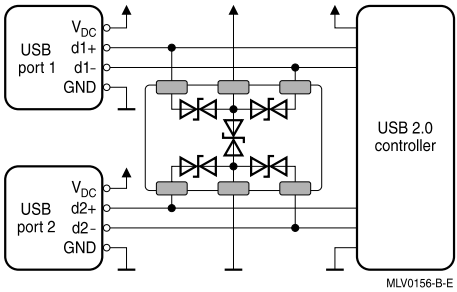


Figure 14

Figures 13 and 14: USB 2.0 dual port protection with high-speedarray CDA6C05GTH

USB compliance test

Representative of other CeraDiodes that have passed the USB compliance test, refer to the so called eye diagrams shown below of three selected types.

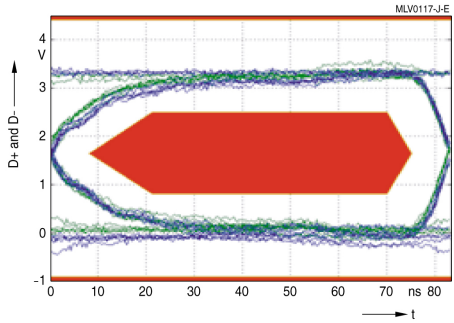


Figure 15: Full-speed measurement (12 Mbit/s) with CDS4C12GTA

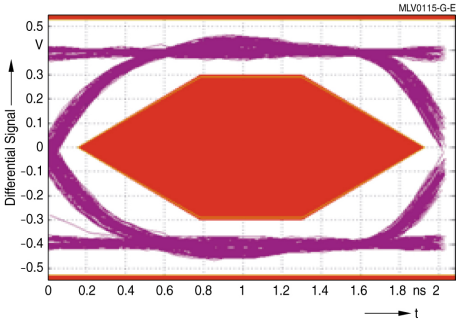


Figure 16: High-speed measurement (480 Mbit/s) with CDS2C16GTH

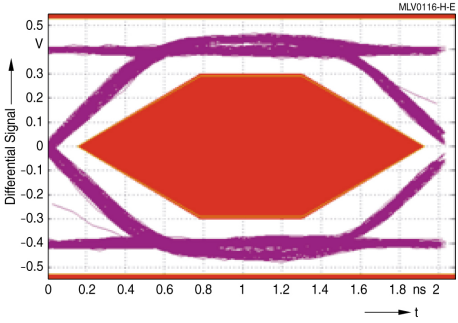


Figure 17: High-speed measurement (480 Mbit/s) with CDA6C05GTH

3 IEEE 1394 (Firewire, DV)

IEEE 1394 interfaces are better known as Firewire connectors in computers or as DV digital connectors between camcorders and DVD recorders. There are two versions with six and four lines respectively. Their data transfer rate of 400 Mbit/s is comparable to that of USB 2.0. The new standard specifies a data rate of 800 Mbit/s (IEEE 1394b).

For suitable CeraDiodes, see chapter "Application matrix".

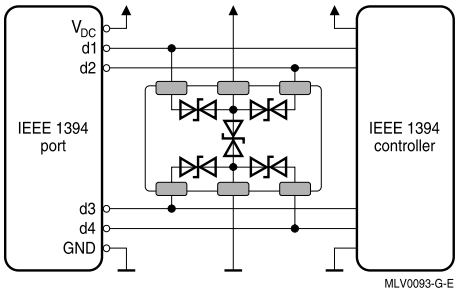


Figure 18: IEEE 1394 line protection with high-speed array CDA6C05GTH

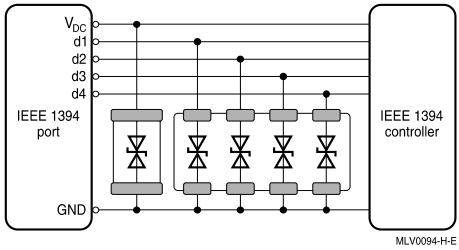


Figure 19: IEEE 1394 line protection with single (e.g. CDS3C15GTA) and array (CDA5C16GTH) CeraDiodes

4 Ethernet

The 10/100/1000 Ethernet is standard for LAN connections.

Requirements of the CeraDiode:

- ESD protection for high-speed data according to IEC 61000-4-2, level 4
- Very low capacitance to prevent signal distortion

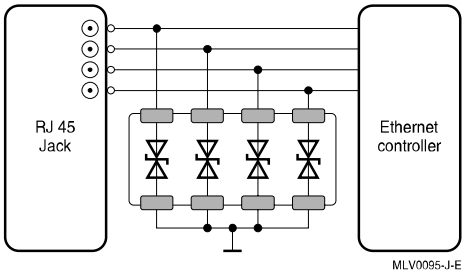


Figure 20: Protection with CeraDiode array (e.g. CDA5C16GTH)

For suitable CeraDiodes, see chapter "Application matrix".

5 DVI and HDMI

With the advent of flat panel displays (LCD and plasma), DVI and HDMI have become established as the digital audio and video interfaces between computers and monitors (DVI) and between DVD players/recorders, set-top boxes, etc. and TV sets (HDMI). Their high-frequency operation requires a very low/an ultra-low line capacitance to avoid signal distortion.

For suitable CeraDiodes, see chapter "Application matrix".

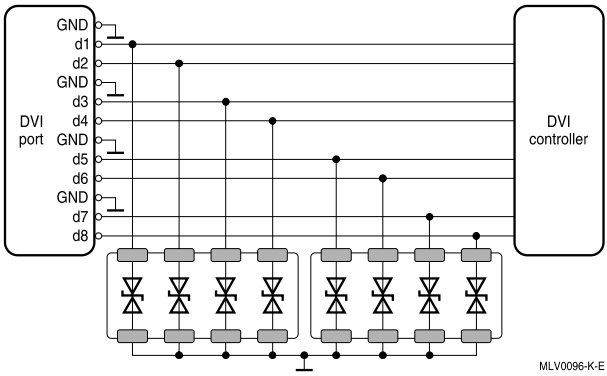


Figure 21: DVI line protection with two arrays

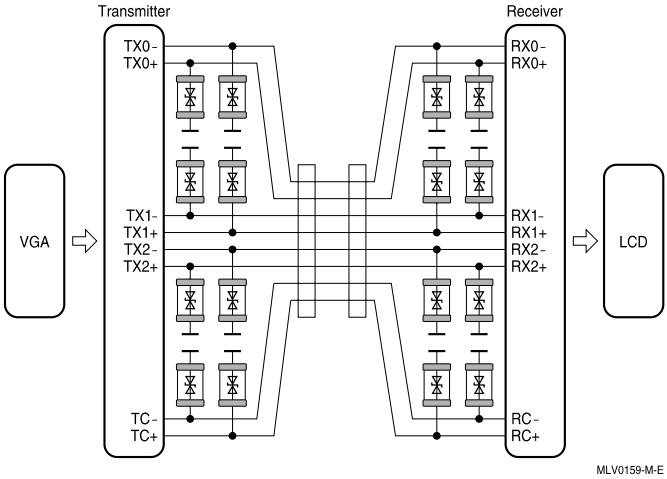


Figure 22: DVI/HDMI line protection with CDS2C05HDMI1

HDMI 1.3a compliance test

The purpose of this test is to ensure that ESD protection components only minimally degrade the differential transmission signal so that it can be properly detected as such in the terminal after transmission. In the test the mask is moved to the left until it is violated, i.e. the signal touches the mask. Then the signal jitter is calculated. The HDMI 1.3a specification requires that the calculated data jitter be less than 0.3 x T_{BIT} . A data jitter of 0.05 x T_{BIT} was demonstrated in the test performed for the CeraDiode CDS2C05HDMI1.

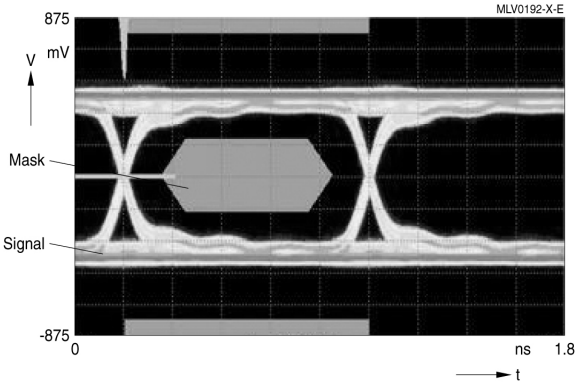


Figure 23 : HDMI 1.3a compliance test result (eye diagram) of CDS2C05HDMI1

Differential transmission links used for high-speed data transfer are very sensitive in terms of impedance matching. If only a small parasitic capacitance (e.g. ESD protection component) is added to the line, the total impedance reduces. According to the HDMI Compliance Tests Specification (CTS) the HDMI receiver ports require a differential impedance of 100 Ω ±15%. Time domain reflectometry is used to measure the impedance. Figure 24 shows that the impedance (see the grey area, position of the ESD protection component on the board) is within the specified band.

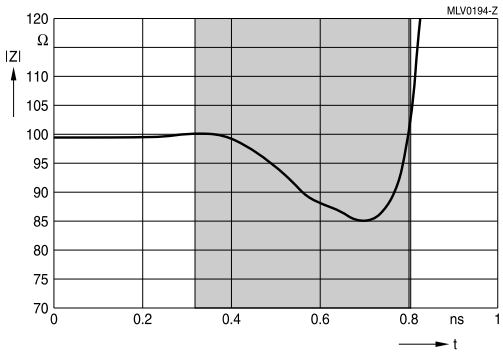


Figure 24: HDMI 1.3a compliance test result (impedance measurement) of CDS2C05HDMI1

6 Other applications

6.1 SIM card

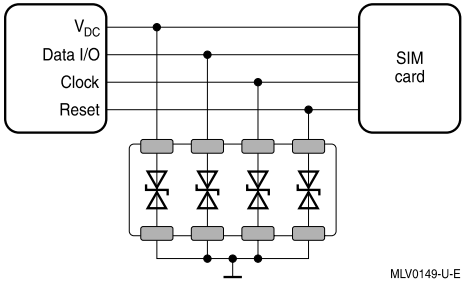


Figure 25: SIM card protection with a CeraDiode (e.g. CDA5C16GTH)

6.2 Keypads, keyboards, pushbuttons

In addition to connectors, pushbuttons offer another access route into the sensitive electronics of a TV set, DVD player, etc. Electrostatic discharge may consequently strike through them when they are touched and destroy the electronics inside. Therefore it is imperative to protect pushbutton lines (about 10 up to 100 kΩ), including channel up/down and sound volume up/down lines connected to a microcontroller IC.

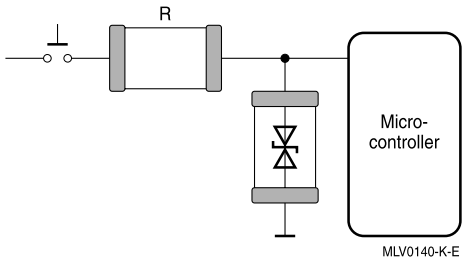


Figure 26: Pushbutton line protection with a CeraDiode

For suitable CeraDiodes, see chapter "Application matrix".

6.3 IR line of preamplifier

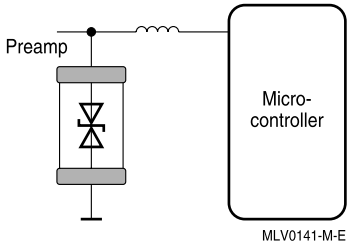


Figure 27: Protecting the IR line of the preamplifier with a CeraDiode

CeraDiodes, e.g.:

- Single 0603 CDS3C20GTA
- Single 1003 CDS4C12GTA

6.4 RF inputs / outputs

The protection device should have very low capacitance and insertion loss.

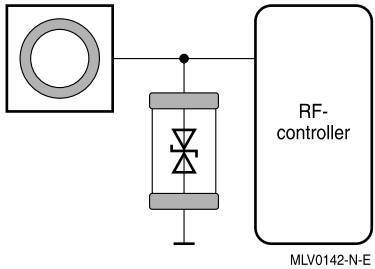


Figure 28: RF controller protection with a CeraDiode

CeraDiodes, e.g.:

- Single 0402 CDS2C16GTH
- Single 0603 CDS3C16GTH

6.5 LCD data line

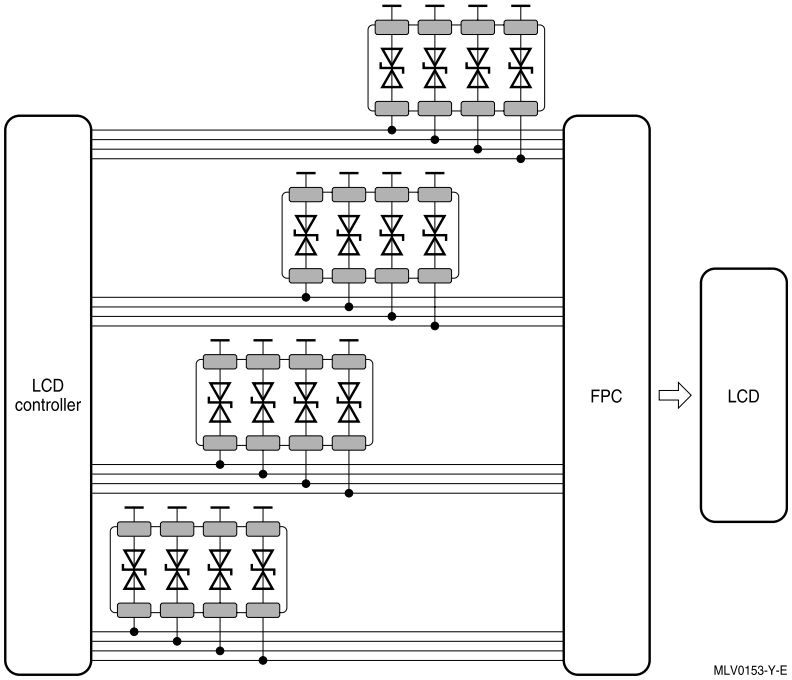


Figure 29: Space-saving ESD protection of LCD data lines with a CeraDiode array

6.6 Drives (e.g. CD, DVD, hard disk, etc.)

For suitable CeraDiodes, see chapter "Application matrix".

6.7 Docking station and cradles

Docking stations and cradles are widely used for portable devices such as PDAs, MP3 players, notebooks, etc. The docking station and cradle is the primary connection for both the data transfer between the portable device and the host computer and for charging the battery.

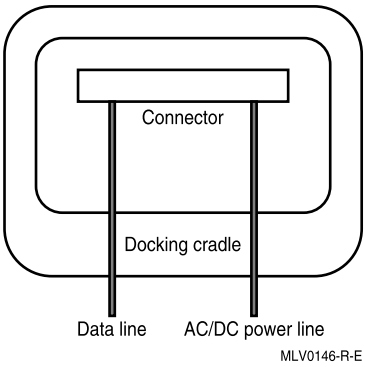


Figure 30: Block diagram of docking station / cradle for portable devices

CeraDiodes for data line protection depend on the type of connection (USB, Ethernet, Firewire, etc.). CeraDiodes for these kind of data lines see chapter "Application matrix".

Corporate goals

Our aim is to play a leading role among the world's most competitive companies in the sector of electronic components. This aim is shared by the EPCOS quality and environment management system:

1 EPCOS quality system

1.1 Extract from EPCOS quality policy

- The quality of our products and services represents a key constituent of our corporate strategy, whose principal aim is customer satisfaction.
- Our quality management system is continuously oriented to the international standards that stipulate the highest requirements.

1.2 Quality management system

The quality management system to ISO/TS 16949:2002 is applied throughout the company and is used to implement the EPCOS quality policy. The implications include:

- As a rule, product and process developments follow the rules of APQP[1)].
- Quality tools such as FMEA[2)], DoE[3)] and SPC[4)] minimize risks and ensure continuous improvements in conjunction with regular internal audits and QM reviews.

1.3 Certification

The EPCOS quality management system forms the basis for the certification according to ISO 9001:2000 and ISO/TS 16949:2002. The certificates are posted on the EPCOS internet (www.epcos.com).

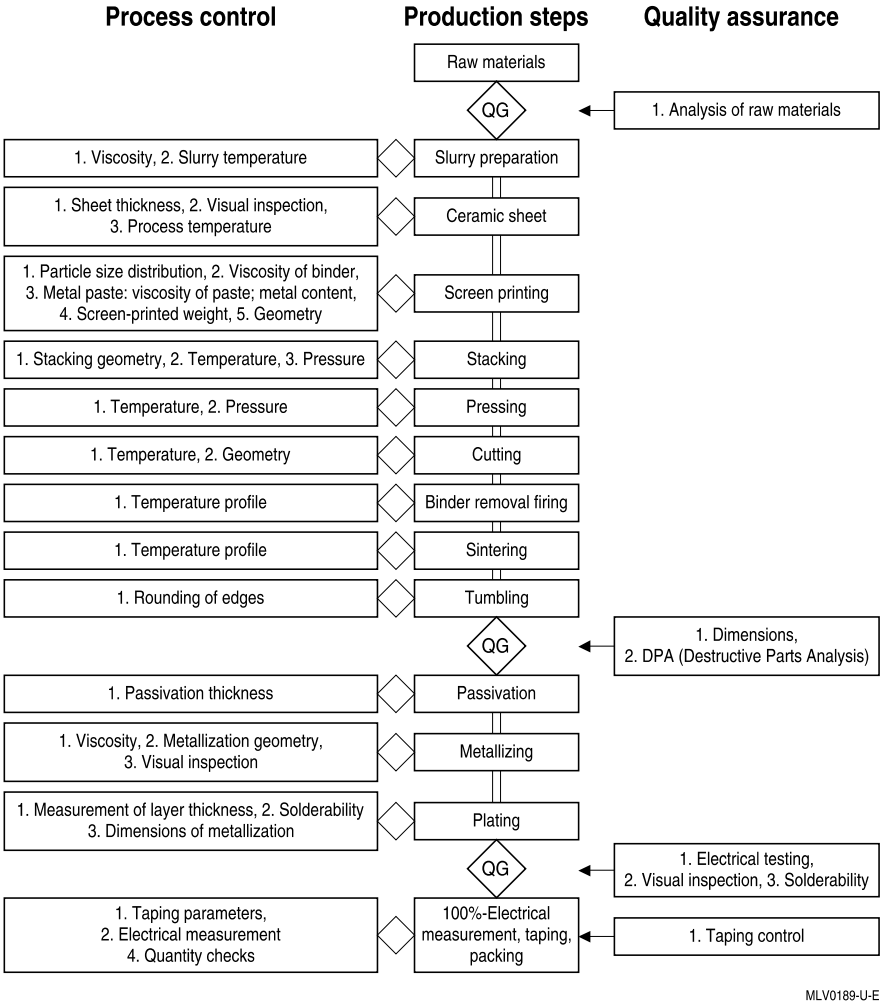
1.4 Production sequence and quality assurance

The business units implement the corporate specifications for quality management in procedural and work instructions referred to products and processes.

The following example shows quality assurance applied to the production sequence of CeraDiodes.

1) APQP = Advanced Product Quality Planning
2) FMEA = Failure Modes and Effects Analysis
3) DoE = Design of Experiments
4) SPC = Statistical Process Control

Manufacturing process and quality assurance of CeraDiodes



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1.5 Delivery quality

"Delivery quality" means compliance with the agreed data at the time of delivery.

1.6 Failure criteria

A component is defective if one of its features does not correspond to the specification of the data sheet or an agreed delivery specification.

1.7 Final inspection / approval for shipment

Final inspection verifies the major properties of the end products batch by batch, usually by means of fully automated selection tests.

Approval for shipment helps certify that products shipped comply with specifications. It includes

- testing of principal parameters,
- identification check and visual assessment,
- examination of papers accompanying the batch.

1.8 Duration of use

The duration of use in terms of reliability is the time period during which random failures occur, i.e. the range in the product operating life in which the failure rate remains largely constant (early failures and end of operating life excepted). The value depends strongly on conditions of use.

1.9 Reliability

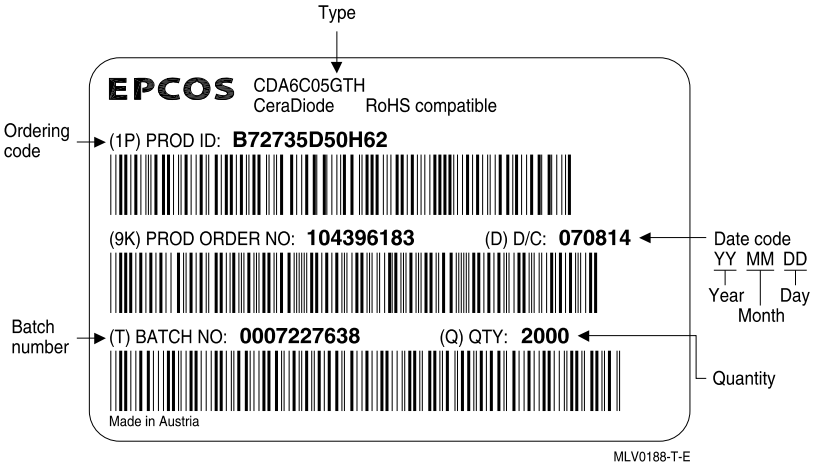
A variety of endurance tests and environmental tests are conducted to assure the reliability of CeraDiodes. These tests are derived from the extremes of expected application conditions, with test conditions intensified to obtain authoritative results within a reasonable period.

The reliability testing programs of EPCOS are based on the test plans of international standards and customer requirements.

EPCOS performs reliability tests to qualify new component families and for periodic requalification.

1.10 Bar code label

The packing of all EPCOS components bears a bar code label stating the type, ordering code, quantity, date of manufacture and batch number. This enables a component to be traced back through the production process, together with its batch and test report.



1.11 Conditions of use

EPCOS products may only be used in line with the technical specifications and assembly instructions and must comply with the state of the art. Non-observance of limits, operating conditions or handling guidelines can lead to disturbances in the circuit and other undesirable consequences such as a higher failure rate.

In this connection, please note the “Important notes” on page 2.
Should you have any application-referred questions, please contact our experts, who will be pleased to advise you.

1.12 Customer complaints

If a fault occurs in a product despite careful manufacture and testing, please contact your local sales organization. They will register your complaint as an RMA[5)] process and forward it to the relevant technical departments for rapid handling.

5) RMA = Return of Material Authorization

EPCOS treats technical complaints according to the 8D methodology; i.e. with the use of interdisciplinary teams who aim to implement rapid countermeasures and sustained corrections and answer all complaints with an 8D report (8D = 8 disciplines).

In order to be able to deal quickly and smoothly with complaints, the following data is helpful:

- Number of components subject to complaint or returned
- Fault description
- How and when was the fault detected?
- Logistics data (date code, batch no., delivery note no.)
- Operating conditions
- Operating duration up to occurrence of the fault
- Measurement parameters in the case of divergent technical data

In the event of transport damage, we would ask you to describe this in more detail and if required to mark it so that it can be distinguished from any further damage sustained during the return shipment. The original package should also be checked and any damage to it described. In order to avoid further damage, the original packaging should also be used for the return shipment.

2 Environmental management system

2.1 Environmental policy

Our fundamental commitment to environmental protection is laid down in the EPCOS environmental policy.

EPCOS defines the following environmental protection principles:

- Above and beyond statutory and administrative requirements, we are continuously working to minimize the burden on the environment and to reduce consumption of energy and natural resources.
- We are taking all precautions necessary to protect our environment against damage.
- Potential impact on the environment is assessed and incorporated in product and process planning at the earliest possible stage.
- Our environmental management system ensures that our environmental protection principles are effectively put into practice. The technical and organizational procedures required are regularly monitored and updated.
- Each employee is required to act in an environmentally conscious manner. It is the constant duty of management to increase and encourage awareness of responsibility at all levels.
- We work with our business partners to promote conformity with similar objectives. We supply our customers with information on ways to minimize any potentially adverse environmental impacts of our products. We work in a spirit of cooperation with the relevant authorities.
- We inform the public of the impact on the environment caused by the company and our activities related to the environment.

2.2 Environmental management system

The EPCOS environmental management system according to ISO 14001 that is applied across the company is used to implement the EPCOS environmental policy. It is posted on the EPCOS intranet and is thus accessible to all employees.

2.3 Certification

The EPCOS environmental management system forms the basis for the ISO 14001 company certification in which all the plants are being successively integrated.
The company certificate is posted on the EPCOS internet (www.epcos.com).

2.4 RoHS

The term “RoHS-compatible” shall mean the following:

The components described as “RoHS-compatible” are compatible with the requirements of the regulations listed below (“Regulations”) and with the requirements of the provisions which will result from transformation of the Regulations into national law to the extent such provisions reflect the Regulations.

- Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment ("Directive 2002/95/EC")
- Commission Decision of 18 August 2005 amending Directive 2002/95/EC (2005/618/EC)
- Commission Decision of 13 October 2005, of 21 October 2005 and of 21 April 2006 amending the Annex to Directive 2002/95/EC (2005/717/EC; 2005/747/EC; 2006/310/EC; 2006/690...692/EC)

2.5 Banned and hazardous substances in components

As a manufacturer of passive components, we develop our products on the basis of the relevant standards and laws and thus ensure that they remain free of materials and substances defined as banned and not exempted by the relevant legislation.

In order to guarantee a standardized procedure for EPCOS worldwide, a mandatory list of banned substances and substances of special interest is part of our environmental management system. The planning and development instructions include regulations and guidelines that aim to identify environmental aspects and to optimize products and processes with respect to material use and environmental compliance, to design them with sparing use of resources and to substitute hazardous substances as far as possible.

Consideration of the environmental aspects is checked and recorded in the design reviews: the environmental officer provides support in the assessment of the environmental impacts of a development project.

2.6 Material data sheets for product families

EPCOS posts material data sheets on the Internet (www.epcos.com/material) that show typical compositions of product groups by selected representatives. The materials are listed with their percentage weight distribution referred to the respective component.

As usual, all materials with a weight percentage exceeding 0.1 are listed. All specifications are typical data and may vary within a product class or production lot.

The material data sheets do not represent assured properties within the scope of the relevant legislation, but are merely given for purposes of information.

Please note in this connection the "Important notes" on page 2.

2.7 Disposal

The specifications given under the header of hazardous substances imply that all the components presented here can generally be disposed off or recycled together with customary electronic waste. However as disposal is regulated by national law, the respective national provisions have to be observed.

General

Some parts of this publication contain statements about the suitability of our CeraDiodes for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CeraDiodes in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CeraDiodes for a particular customer application. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CeraDiodes with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use EPCOS CeraDiodes for purposes not identified in our specifications, application notes and data books.
- Ensure the suitability of a CeraDiode in particular by testing it for reliability during design-in. Always evaluate a CeraDiode under worst-case conditions.
- Pay special attention to the reliability of CeraDiodes intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

Design notes

- Always connect a CeraDiode in parallel with the electronic circuit to be protected.
- Consider maximum rated power dissipation if a CeraDiode has insufficient time to cool down between a number of pulses occurring within a specified isolated time period. Ensure that electrical characteristics do not degrade.
- Consider derating at higher operating temperatures. Choose the highest voltage class compatible with derating at higher temperatures.
- Surge currents beyond specified values will puncture a CeraDiode. In extreme cases a CeraDiode will burst.
- If steep surge current edges are to be expected, make sure your design is as low-inductance as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. Do not use CeraDiodes in applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraDiodes that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraDiodes in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures like thermal fuses.

Storage

- Only store CeraDiodes in their original packaging. Do not open the package before storage.
- Storage conditions in original packaging: temperature -25 to +45°C, relative humidity ≤75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraDiodes where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CeraDiodes may stick together, causing problems during mounting.
- Avoid contamination of the CeraDiode surface during storage, handling and processing.
- Avoid storing CeraDiodes in harmful environments where they are exposed to corrosive gases for example (SO_x, Cl).
- Use CeraDiodes as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraDiodes after shipment from EPCOS within the time specified: 12 months.

Handling

- Do not drop CeraDiodes and allow them to be chipped.
- Do not touch CeraDiodes with your bare hands - gloves are recommended.
- Avoid contamination of the CeraDiode surface during handling.

Mounting

- When CeraDiodes are encapsulated with sealing material or overmolded with plastic material, be sure to observe the precautions in “Mounting instructions”, “Sealing, potting and overmolding”.
- Make sure an electrode is not scratched before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraDiodes are clean before mounting.
- The surface temperature of an operating CeraDiode can be higher. Ensure that adjacent components are placed at a sufficient distance from a CeraDiode to allow proper cooling.
- Avoid contamination of the CeraDiode surface during processing.
- Only CeraDiodes with an Ni barrier termination are approved for lead-free soldering.

Soldering

- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.

Operation

- Use CeraDiodes only within the specified operating temperature range.
- Use CeraDiodes only within specified voltage and current ranges.
- Environmental conditions must not harm a CeraDiode. Only use them in normal atmospheric conditions. Reducing the atmosphere (e.g. hydrogen or nitrogen atmosphere) is prohibited.
- Prevent a CeraDiode from contacting liquids and solvents. Make sure that no water enters a CeraDiode (e.g. through plug terminals).
- Avoid dewing and condensation.
- EPCOS CeraDiodes are designed for indoor applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content
- EPCOS CeraDiodes are not suitable for switching applications or voltage stabilization where static power dissipation is required.
- CeraDiodes are designed for ESD protection only.

This listing does not claim to be complete, it merely reflects the experience of EPCOS AG.

Symbols and terms

CeraDiode	Semiconductor diode	
C_{typ}		Typical capacitance
I_{BR}	I_R, I_T	(Reverse) current @ breakdown voltage
I_{leak}	I_{RM}	(Reverse) leakage current
I_{PP}	I_{PP}	Current @ clamping voltage
I_{PP}	I_P, I_{PP}	Peak pulse current
P_{PP}	P_{PP}	Peak pulse power
T_{op}		Operating temperature
T_{stg}		Storage temperature
V_{BR}	V_{BR}	(Reverse) breakdown voltage
$V_{BR,min}$		Minimum breakdown voltage
V_{clamp}	V_{cl}, V_C	Clamping voltage
$V_{clamp,max}$		Maximum clamping voltage
V_{DC}	V_{RM}, V_{RWM}, V_{WM}, V_{DC}	(Reverse) stand-off voltage, working voltage, operating voltage
$V_{DC,max}$		Maximum DC operating voltage
$V_{ESD,air}$		Air discharge ESD capability
$V_{ESD,contact}$		Contact discharge ESD capability
V_{leak}	V_{RM}, V_{RWM}, V_{WM}, V_{DC}	(Reverse) voltage @ leakage current
- *)	I_F	Current @ forward voltage
- *)	I_{RM}, $I_{RM,max}$@V_{RM}	(Reverse) current @ maximum reverse stand-off voltage, working voltage, operating voltage
- *)	V_F	Forward voltage

*) Not applicable due to bidirectional characteristics of CeraDiodes

S

T

U

V

W

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